Modeling of the static and dynamic behavior of differential drivers

Modeling of the Static and Dynamic Behavior of Differential Drivers

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Abstract – *The development of behavioral models of differential drivers for the simulation of signal integrity and electromagnetic compatibility problems is addressed. The obtained macromodels are readily included in any circuit simulation environment. A complete modeling example is given.*

1 INTRODUCTION

Low Voltage Differential Signaling (LVDS) is going to establish as the dominant standard for on-board and off-board high-performance data links [1, 2, 3]. It allows extremely high data rates, on the order of one Gbps, along with reduced EMI effects and reduced power absorption.

In order to simulate the operation of LVDS link for the assessment of Signal Integrity (SI) and ElectroMagnetic Compatibility (EMC) problems, suitable behavioral models (or macromodels) of differential drivers and receivers are needed. To this aim, in this paper, we address the behavioral modeling of LVDS differential driver output buffers. The proposed modeling procedure exploits piecewise models and parametric relations introduced in [4] for single-ended devices, and is demonstrated by a complete modeling example.

2 DEVICE AND MODEL STRUCTURE

The output buffers of LVDS drivers operate via current steering techniques, as shown in Fig. 1. Two voltage controlled current source devices are used to provide the current sent to and drawn from resistor R_r at receiver input terminals. When switches A are closed, i_r is positive, whereas when switches B are closed i_r is negative and the voltage across receiver input terminals changes polarity. In actual applications, output buffers may contain matching resistors across the output terminals and control subcircuits to ensure proper output current and voltage values over possible process, supply voltage and temperature variations.

In fixed logic state, the ideal LVDS output buffer of Fig. 1 can be considered as a three-terminal circuit element characterized by constitutive relations of the form

$$\begin{cases} i_1 = i_{1H}(v_1, v_2) \\ i_2 = i_{2H}(v_1, v_2) \end{cases} \quad \begin{cases} i_1 = i_{1L}(v_1, v_2) \\ i_2 = i_{2L}(v_1, v_2) \end{cases} \tag{1}$$

where H and L denote the HIGH and LOW logic state, respectively, and the output currents are allowed to be functions of both voltages to take into account variants of the buffer basic scheme with internal resistor and control circuits. A complete macromodel describing state switching

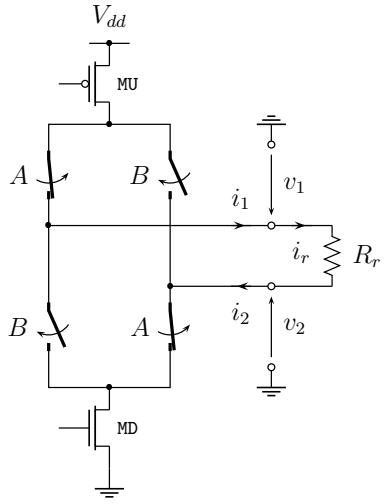

Figure 1: Generic structure of a LVDS driver and its relevant electric variables.

from steady state operation can be obtained by combining in a two-piece model the constitutive relations (1) (submodels) by means of time-varying weighting coefficients

$$\begin{cases} i_1 = w_{1H}(t) i_{1H}(v_1, v_2) + w_{1L}(t) i_{1L}(v_1, v_2) \\ i_2 = w_{2H}(t) i_{2H}(v_1, v_2) + w_{2L}(t) i_{2L}(v_1, v_2) \end{cases} \tag{2}$$

When suitable submodels are available for terminal currents in fixed logic states ($i_{1H}(v_1, v_2)$, ...), the weighting coefficients can be obtained from the device responses during switching experiments. The problem is then to devise and estimate the parameters of suitable relations for submodels (1). A straightforward approach is to represent i_{nH} and i_{nL}, $n = 1, 2$ by a sum of a static mapping and a (possibly parametric) contribution taking into account dynamic effects [4]. Both the static mapping and the dynamic contribution can be estimated from currents caused by suitable test sources connected to driver output terminals, like in Fig. 2. The static mappings easily arise from steady state current values, whereas transient responses help the estimation of dynamic contributions. Of course, the terminal voltage variations applied by test sources should correspond to differential and common mode voltage variations within limits specified by the LVDS standard. Besides, for output buffers containing control circuits, voltage test sources should be properly replaced by sources compatible with the static characteristics of those devices (*e.g.*, see [5, 6, 7] for details on the possible implementation of control circuits).

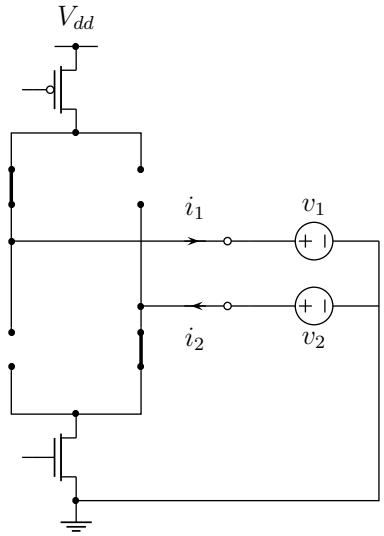

Figure 2: Common setup for both the estimation of the static characteristics and the dynamic behavior of the LVDS device of Fig. 1 in the HIGH logic state.

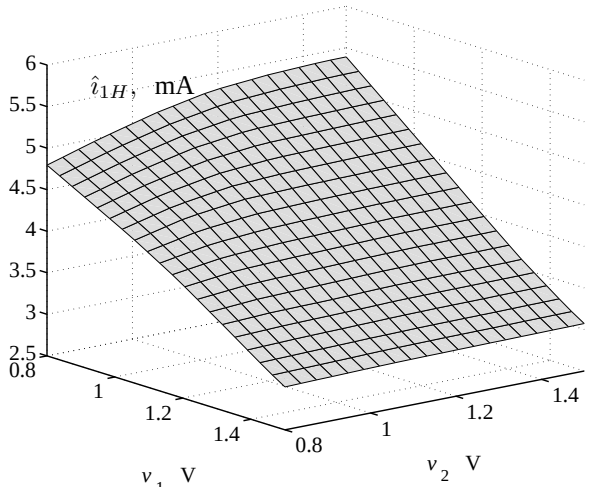

Figure 3: Static characteristic $\hat{\imath}_{1H}(v_1, v_2)$ of the current i_1 for the example driver forced in the HIGH logic state.

3 NUMERICAL EXAMPLE

In this Section, the proposed modeling approach is demonstrated on a commercial device. The modeled device is the Fairchild FIN1001 3.3. V LVDS High Speed Differential Driver, whose HSPICE encrypted transistor-level model (available from the official website `www.fairchildsemi.com`) is assumed as the *reference* model hereafter. All the simulations are performed by using HSPICE and the reference model is used for both the computation of the responses needed for the estimation of macromodel parameters and for its validation.

For this example driver, submodels i_{nH} and i_{nL}, $n = 1, 2$ are sums of a static and a dynamic part, where the dynamic part is sought for within the subclass of linear parametric models. The assumption of the linear dynamic part arises from the observation of a nearly linear and capacitive dynamic behavior of the driver operating in fixed logic state. As an example, for $i_{nH},\ n = 1, 2$ of Eq. (2), the model representation turns out to be defined by

$$\begin{cases} i_{1H} = \hat{\imath}_{1H}(v_1, v_2) - C_{1H}\frac{dv_1}{dt} - C_{12H}\frac{d(v_1 - v_2)}{dt} \\ i_{2H} = \hat{\imath}_{2H}(v_1, v_2) + C_{2H}\frac{dv_2}{dt} + C_{12H}\frac{d(v_2 - v_1)}{dt} \end{cases} \quad (3)$$

where $\hat{\imath}_{1H}$ and $\hat{\imath}_{2H}$ are the static characteristic of currents i_1 and i_2 for the driver forced in the fixed HIGH logic state. As an example, Fig. 3 shows the static characteristic $\hat{\imath}_{1H}(v_1, v_2)$.

It is worth noting that the model representation (3) used for this modeling example is similar to the one recommended by the IBIS standard [8]. Representation (3), however, includes both static and dynamic coupling effects between the terminal variables. This approach is more general and does not significantly affect the complexity of the resulting macromodel. Decoupled static characteristics, *i.e.*, $i_{1H} = i_{1H}(v_1)$ and $i_{2H} = i_{2H}(v_2)$, assume weak influence of the neglected voltage variables, that is not guaranteed. Besides, even when this approximation holds, the measurement of a decoupled static characteristic should be performed by keeping the neglected voltage variable close to values expected during operation [9].

The estimation of the dynamic contribution is carried out by recasting Eq. 3 as a linear least square problem for $\{C_{1H}, C_{12H}, C_{2H}\}$ and $\{C_{1L}, C_{12L}, C_{2L}\}$. This is achieved by recording the device responses $i_1(t)$ and $i_2(t)$ while the driver is forced in the HIGH or LOW logic state and the terminals are connected to noise voltage sources as in Fig. 2. In this example, independent gaussian noise sources with mean value equal to the nominal common mode voltage $\frac{(v_1+v_2)}{2} = 1.25\,\mathrm{V}$ and standard deviation $10\,\mathrm{mV}$ are used. In addition, the linearity of the dynamic contribution has been verified by applying noisy signals with amplitude on the order of the full voltage swing specified by the LVDS standard. The values of the estimated capacitors are $\{C_{1H}, C_{12H}, C_{2H}\} = \{1.65, 0.125, 1.66\}$ pF and $\{C_{1L}, C_{12L}, C_{2L}\} = \{1.66, 0.109, 1.62\}$ pF.

Finally, the estimation of weighting coefficients are obtained through linear inversion of (2) by means of the reference responses $i_1(t)$, $i_2(t)$, $v_1(t)$, $v_1(t)$ obtained while the device is connected to a $100\,\Omega$ differential resistor and is driven to produce a logic HIGH pulse.

The obtained macromodel is implemented as an HSPICE subcircuit with standard component and validated by two test circuits. The first test circuit is composed of the modeled device driving a $50\,\Omega$ differential resistor with a logic HIGH pulse. For this test case, Fig. 4 shows the reference and macromodel responses of the output terminal voltages $v_1(t)$, $v_2(t)$ and of the differential voltage $v_d(t)$.

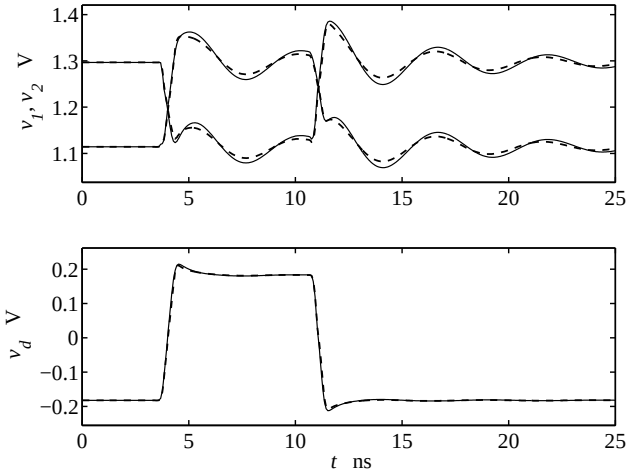

Figure 4: Output port voltages $v_1(t)$, $v_2(t)$ (top panel) and differential voltage $v_d(t)$ (bottom panel) computed for the first test circuit (see text). Solid line: reference, dashed line: macromodel.

The second test circuit is composed of the modeled device driving a coupled transmission line (differential mode impedance $Z_e = 50\,\Omega$, common mode impedance $Z_o = 100\,\Omega$, line length 0.15 m) loaded by a $100\,\Omega$ differential resistor with a logic HIGH pulse. For this test case, Fig. 5 shows the reference and macromodel responses of the output terminal voltages $v_1(t)$, $v_2(t)$ and of the differential voltage $v_d(t)$.

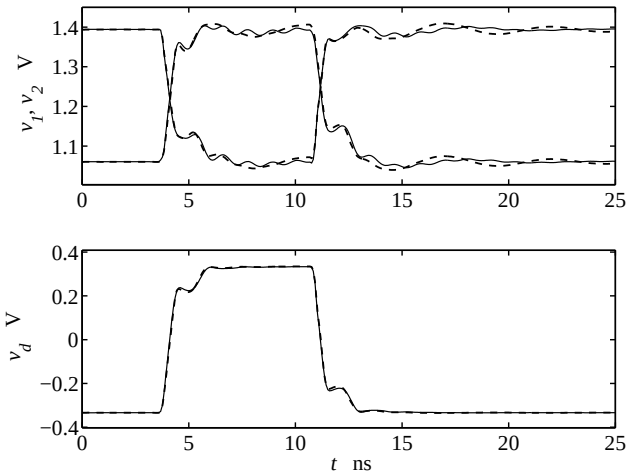

Figure 5: Output port voltages $v_1(t)$, $v_2(t)$ (top panel) and differential voltage $v_d(t)$ (bottom panel) computed for the second test circuit (see text). Solid line: reference, dashed line: macromodel.

The accuracy of the proposed macromodel has been quantified by computing the timing error and the maximum relative voltage error. The timing error is defined as the maximum delay between the reference and the macromodel differential voltage responses measured for the zero voltage crossing. As an example, for the curves of Fig. 4 and Fig. 5 the maximum timing error is 15 ps. The maximum relative voltage error is computed as the maximum error between the reference and macromodel voltage responses divided by the nominal voltage swing of 350 mV. Again, form the same previous validation curves, it turns out to be 5.4%.

Table 1: CPU time and memory usage for the computation of the curves of Fig. 4 by means of HSPICE.

Model	CPU time	Memory
reference	10.70 sec	1430 Kb
macromodel	2.35 sec	490 kb

Finally, macromodel efficiency is assessed by the CPU-time and memory usage required for circuit simulations. For the example device of this Section, Tab. 1 collects the figures of the efficiency comparison between the reference transistor-level model and the macromodel for the computation of the curves of Fig. 4.

Acknowledgements

This work was supported in part by the Italian Ministry of University (MIUR) under a Program for the Development of Research of National Interest (PRIN grant #2002093437) and by CERCOM, Center for Multimedia Radio Communications of the Electronics Dept, Politecnico di Torino.

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